Debugging and Preventing Abnormally High V_{min} During Logic Scan Test Bring-up

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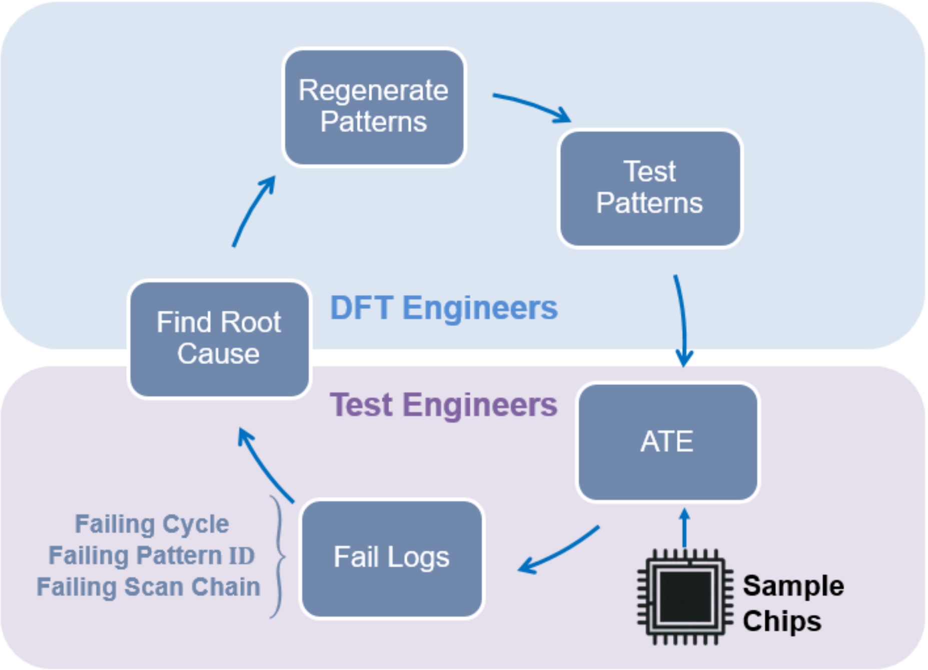
Outline

- Introduction
- Background
- Per-pattern V_{min} Debugging
- Proposed Prevention Methods
- Experimental Results
- Conclusion

Test Bring-up

- **To ensure test specifications are met**
  - Prevent production yield loss
- **Only some sample chips tested**
- **Cooperation of DFT and Test engineers**
  - Many pre-silicon and post-silicon iterations



V_{min} Test

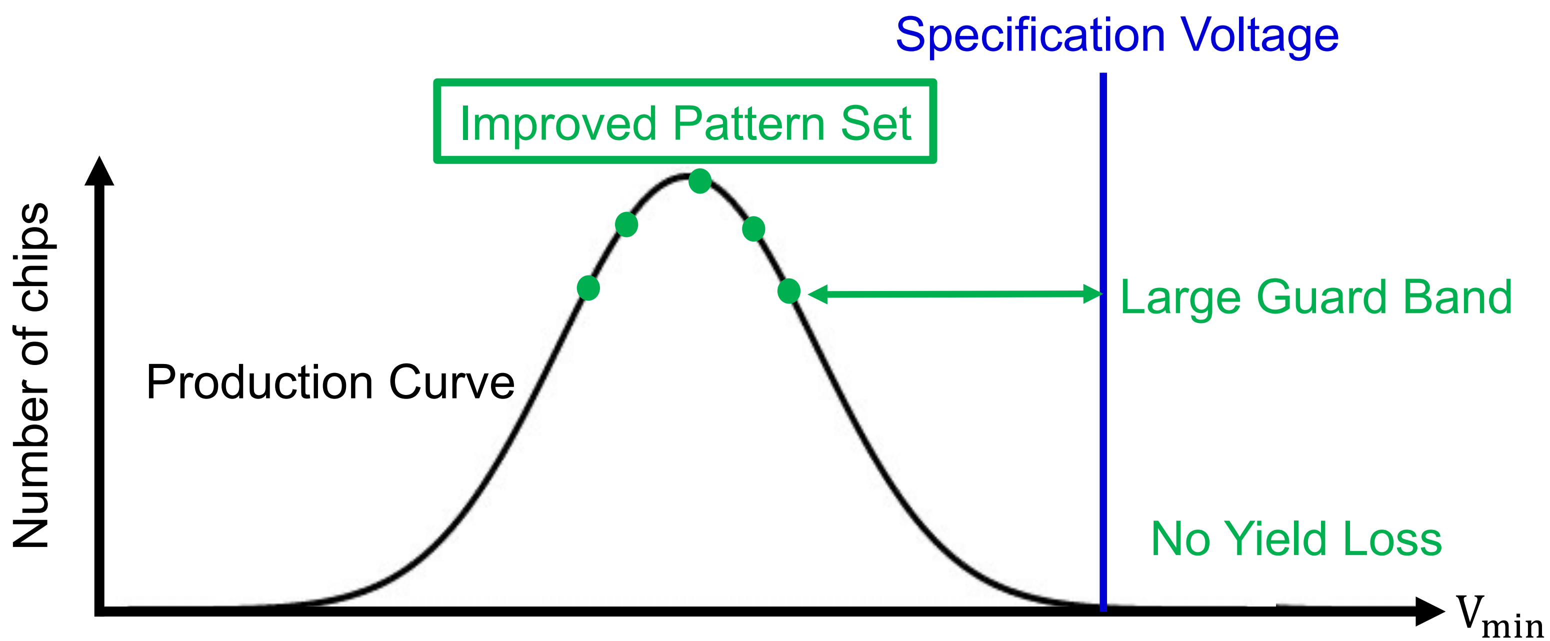
- V_{min}
  - minimum voltage at which a chip passes the test
- **V_{min} is an indicator of chips' performance**
  - Power consumption
  - A specification during test bring-up
- **V_{min} is switching activity dependent**
  - Switching activity of test mode is higher than functional mode
  - Cause yield loss due to over-testing when V_{min} of test mode is much higher

High V_{min} in Test Bring-up

- **High V_{min} of a pattern set**
  - Too close to specification voltage
  - Cause yield loss due to over-testing
  - Usually assumed to be caused by high power
- **Debugging with power-aware ATPG**
  - Generate a low-power pattern set
  - Add constraints to ATPG
    → Need more patterns to reach same fault coverage

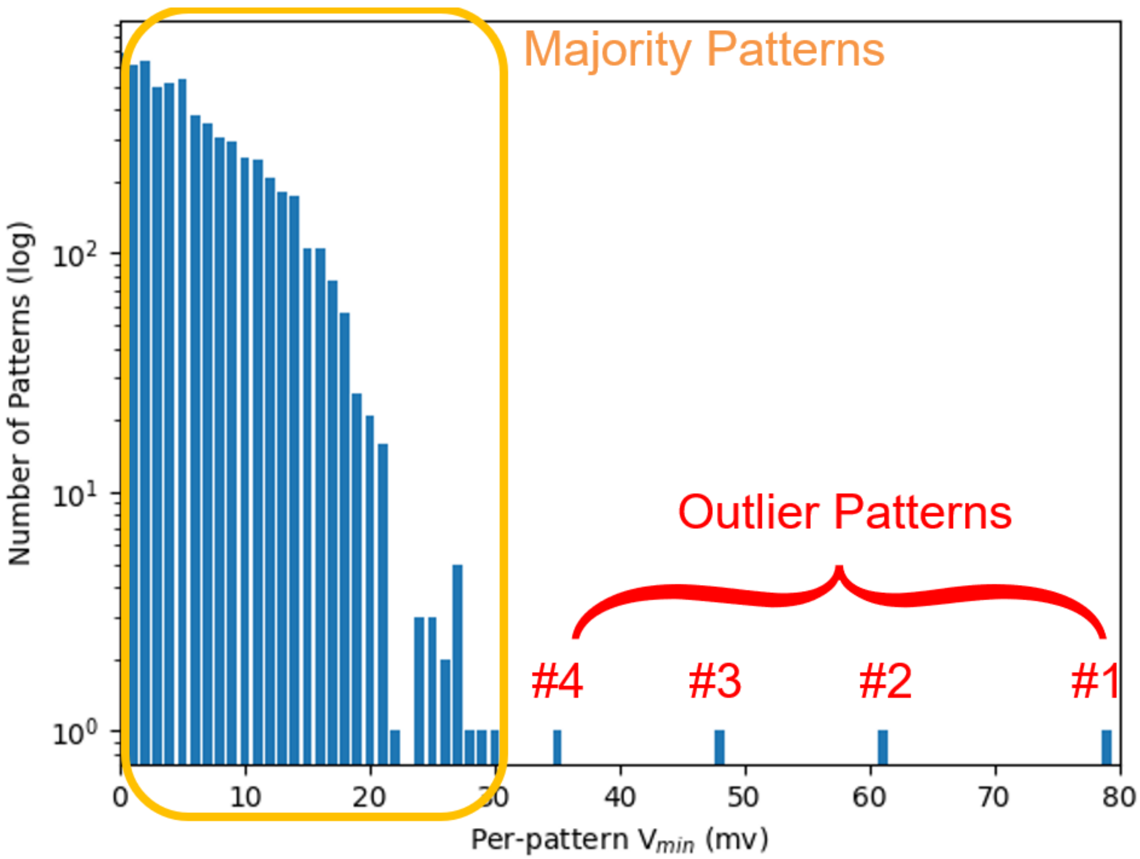
Improve High V_{min} in Test Bring-up

- **Suppose five sample chips in test bring-up**
  - Require large V_{min} guard band



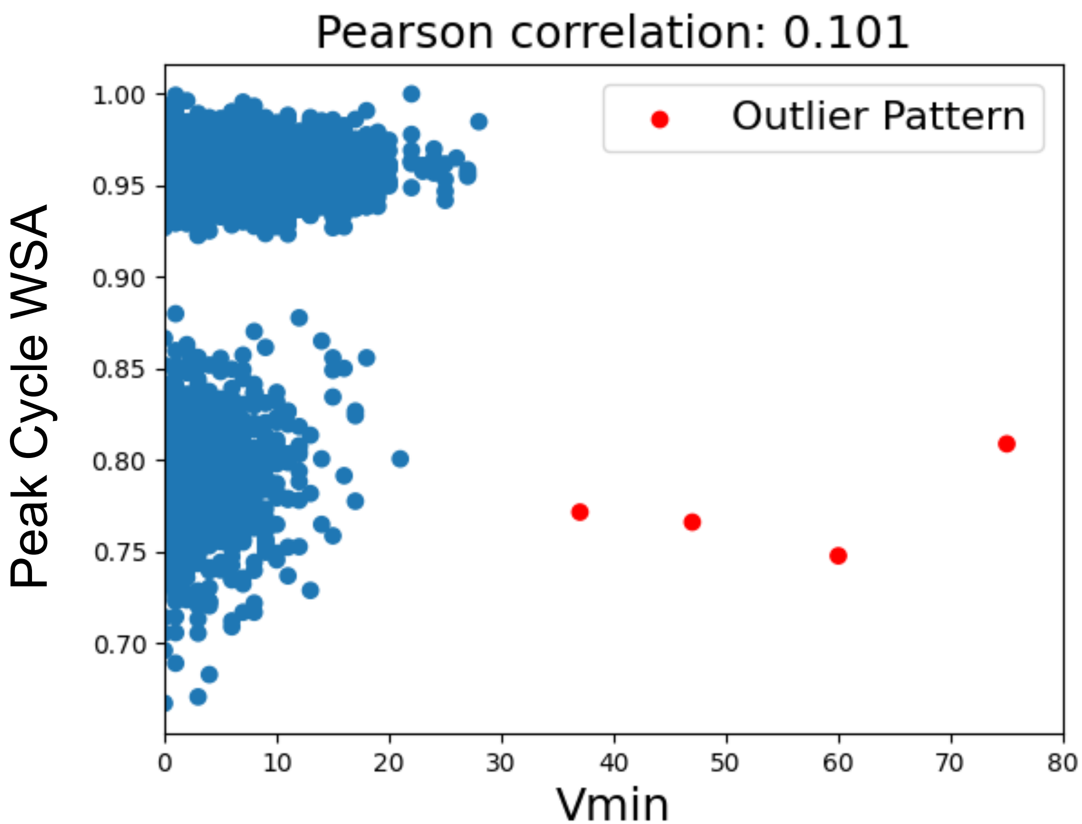
Debugging Case Observation #1

- Some patterns fail at much higher voltages



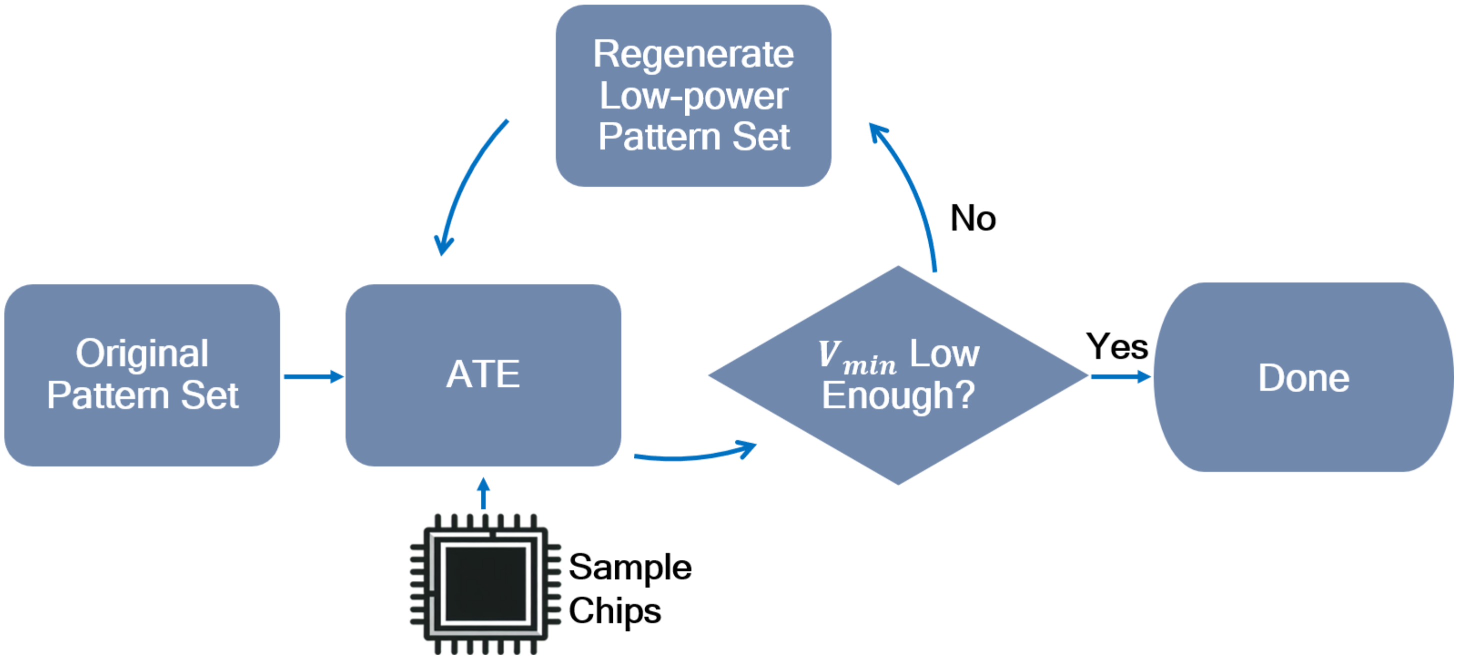
Debugging Case Observation #2

- Low correlation between power and V_{min}



Traditional flow

- Traditional flow to debug high V_{min} pattern set



Many Iterations

Ineffective if root cause is not power

Motivations & Goals

Motivations

- Many iterations in traditional flow
- Ineffective when over-testing is not caused by power
- Pattern count inflation of power-aware ATPG
- Outlier patterns limit the V_{min} of pattern sets

Goals

- Find out the root cause of high V_{min} pattern sets
- Propose a method to improve V_{min}

Contribution & Key Results

Contribution

- Debug a high V_{min} pattern set
  - Diagnosis results and find out the root cause
  - Activated unconstrained paths are the root cause of high V_{min}
- Proposed pre-silicon and post-silicon methods
  - Prevent high V_{min} patterns caused by unconstrained paths

Key Results

- Achieve 28.83mV to 39.33mV V_{min} improvements
- Only 0% to 0.5% pattern count inflation
  - Same fault coverage

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Related Work

- **Understanding Power Supply Droop During At-Speed Scan Testing** [Pant 09]
  - Power supply droop in at-speed scan testing
  - Present over-testing issues during at-speed scan testing

- **Low Capture Power At-Speed Test with Local Hot Spot Analysis to Reduce Over-Test** [Srivastava 22]
  - To solve power-droop induced over-testing issue
  - Consider local WSA for ATPG
  - Require post-silicon data

[Pant 09] P. Pant and J. Zelman, "Understanding Power Supply Droop during At-Speed Scan Testing," 2009 27th IEEE VLSI Test Symposium
[Srivastava 22] A. Srivastava and J. Abraham, "Low Capture Power At-Speed Test with Local Hot Spot Analysis to Reduce Over-Test," 2022 IEEE International Test Conference (ITC)

Related Work

- **A case study of IR-drop in structured at-speed testing** [Saxena 03]
  - High switching activity cause silicon failures for at-speed test
  - Scan test has $^1/_3$ more toggle activity than functional activity

- **Vector-based Dynamic IR-drop Prediction Using Machine Learning** [Chen 22]
  - Propose density map features for IR-drop prediction model
  - Can be used to identify IR risky patterns
  - Most of the features are from RedHawk and cell based
  - No silicon data

[Saxena 03] J. Saxena et al., "A case study of ir-drop in structured at-speed testing," International Test Conference, 2003. Proceedings. ITC
[Chen 22] J. -X. Chen et al., "Vector-based Dynamic IR-drop Prediction Using Machine Learning," 2022 27th Asia and South Pacific Design Automation Conference (ASP-DAC), Taipei, Taiwan

Related Work

- **Applications of Test Techniques for Improving Silicon to Pre-Silicon Timing Correlation** [Jajodia 19]
  - To better correlate STA results to first failing path
  - IR-drop, voltage droop affects correlation of STA and failing path
  - Need HSpice, STA tool, IR-drop simulator

- **Delay Defect Characteristics and Testing Strategies** [Kim 03]
  - False paths can be activated during scan-based delay testing
  - Cause yield loss due to over-testing

[Jajodia 19] R. Jajodia, "Applications of test techniques for improving silicon to pre-silicontiming correlation," in 2019 IEEE International Test Conference India(ITC India)
[Kim 03] Kee Sup Kim, S. Mitra and P. G. Ryan, "Delay defect characteristics and testing strategies," Design & Test of Computers, 2003

Suspected Root Cause of High V_{min}

- **Power supply noise**
  - IR-drop [Saxena 03]
    - Static and dynamic IR drop
    - Cause V_{min} problem during at-speed test
  - Power supply droop [Srivastava 22]
    - Caused by sudden changes in current demand
    - Critical during at-speed test
  - Weighted Switching Activity (WSA) [Basker 12]
    - Indicator to power supply noise (IR-drop & power supply droop)
    - $\sum_{\forall gate} Switch \times (1 + \#gatefanout)$

[Saxena 03] J. Saxena et al., "A case study of ir-drop in structured at-speed testing," International Test Conference, 2003
[Srivastava 22] A. Srivastava and J. Abraham, "Low Capture Power At-Speed Test with Local Hot Spot Analysis to Reduce Over-Test," International Test Conference, 2022
[Basker 12] P. Basker and A. Arulmurugan, "Survey of low power testing of VLSI circuits," International Conference on Computer Communication and Informatics, 2012

Suspected Root Cause of High V_{min}

- **Miscorrelation between static timing analysis and silicon** [Jajodia 19]
  - Timing differences among various voltages
  - STA and failure mismatch
  - Possibly lead to unexpected failures
- **Unconstrained paths (timing exceptions)** [Kim 03]
  - Include false paths and multicycle paths
  - Timing would not be fixed
  - May cause failures if timing-critical and activated

[Jajodia 19] R. Jajodia et al.,"Applications of Test Techniques for Improving Silicon to Pre-SiliconTiming Correlation," International Test Conference India, 2019
[Kim 03] Kee Sup Kim, S. Mitra and P. G. Ryan, "Delay defect characteristics and testing strategies," Design & Test of Computers, 2003

Consider Unconstrained Paths

Synopsys Design Constraint (SDC)

- Used in design process and sign-off
- Containing all unconstrained paths
- Used for PrimeTime

SDC file example

```
set_false_path
–from A -to B

set_false_path
–through C

set_multicycle_path
 –from D -to E

set_multicycle_path
–through F
```

In Tessent

- Read SDC file before generating patterns
- The endpoints of unconstrained paths should be masked
- Not properly masking may lead to unexpected failures

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Debugging Case

- Type of patterns : Transition Delay Fault (TDF)
- At speed : Yes
- Tools : Tessent and PrimeTime
- # of sample chips: 8

Per-pattern V_{min}

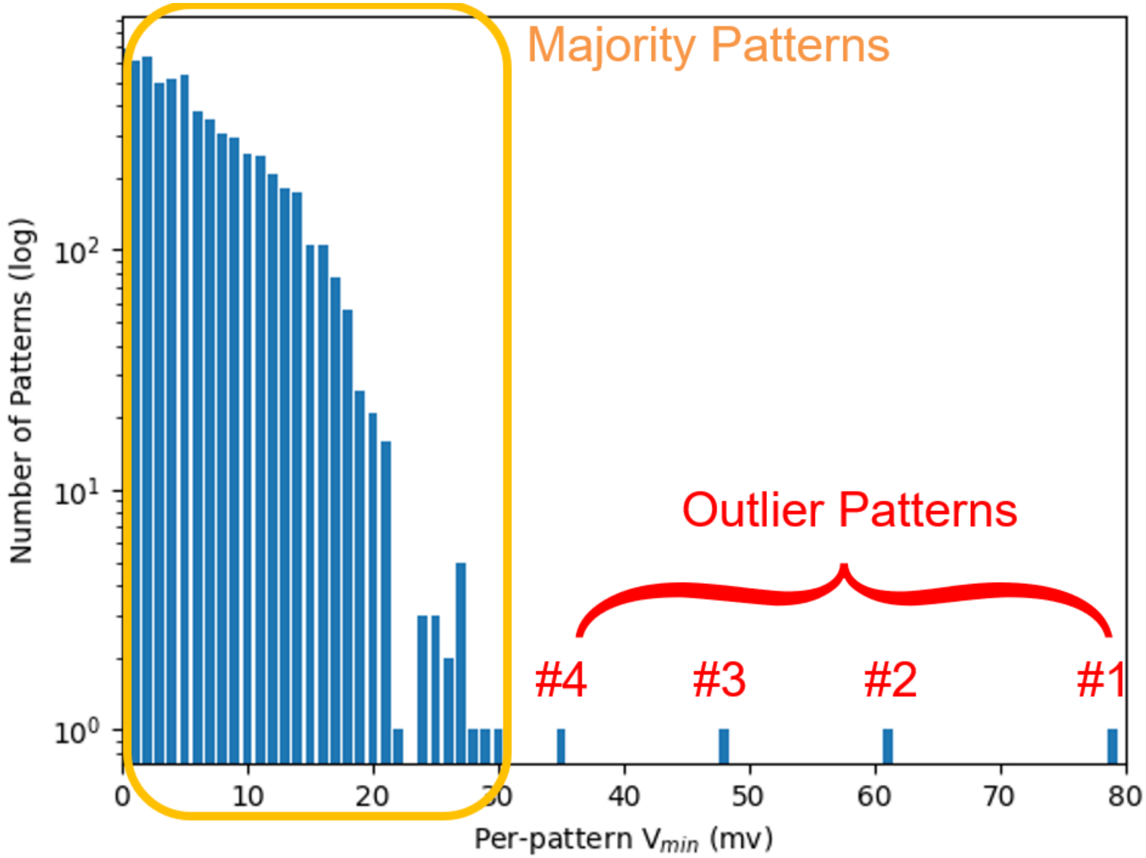
- **V_{min} of each test pattern is different**
  - Some patterns limit V_{min} of a pattern set
- $V_{min}(c, P) = \max_{\forall p \in P} V_{min}(c, p)$
  - c: a chip, P: a pattern set, p: a pattern in P

Pattern ID	$0.96V_{spec}$	$0.97V_{spec}$	$0.98V_{spec}$	$0.99V_{spec}$	V_{spec}
$Pattern_A$					
$Pattern_B$					
$Pattern_C$					
$Pattern_D$					
$Pattern_E$					

Pattern ID	Per−pattern V_{min}(mV)	Pattern-set V_{min}(mV)
$Pattern_A$	V_{spec}	V_{spec}
$Pattern_B$	$0.99V_{spec}$	
$Pattern_C$	$0.97V_{spec}$	
$Pattern_D$	$0.98V_{spec}$	
$Pattern_E$	$0.97V_{spec}$	

Outlier Patterns

- Outlier patterns have abnormally high V_{min}
- Identifying them helps us to debug



Debugging Attempts

- No.1: Power-aware ATPG
- No.2: Global dynamic power
- No.3: Local dynamic power
- No.4: Dynamic power around the long path
- No.5: Unconstrained paths

No.1
Power-aware ATPG

- **Hypothesis:**
  V_{min} decreases as power constraints get stricter
- **Experiment: Power-aware ATPG**
  - Usually used to improve V_{min} by DFT engineers
  - Stricter power constraints → Lower V_{min}
- **Several constraints can be chosen**
  - For capture cycles or shift cycles
  - Peak or Average
  - WSA or state element transition

No.1
Power-aware ATPG

- Choose peak WSA for capture cycles

Pattern Set	Capture WSA_{th}	Pattern-set V_{min} (Shifted)	Outlier Pattern Exist?
PS	None	79	Yes
PS_{15}	15%	46	Yes
PS_{14}	14%	49	Yes
PS_{13}	13%	63	Yes
PS_{12}	12%	47	Yes
PS_{11}	11%	50	Yes
PS_{10}	10%	48	Yes

- Expect: Lower WSA_{th} → Lower V_{min}
- Different constraints lead to similar results
- No direct correlation in our case

No.2
Global Dynamic Power

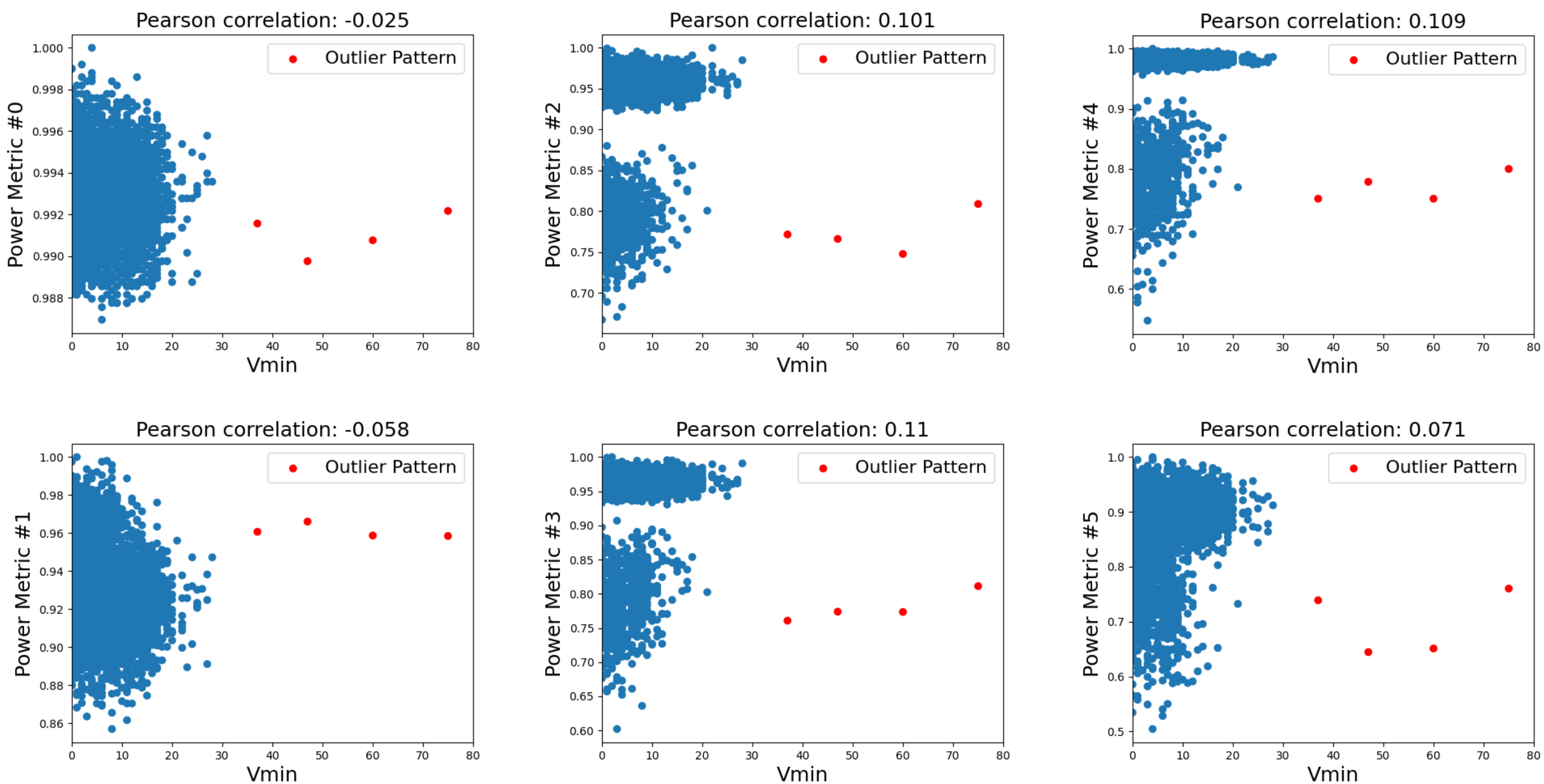
- **Hypothesis:**
  Global dynamic power is correlated to V_{min}
- **Experiment:**
  Calculate per-pattern power metrics
  - Six power metrics from Tessent
  - Considered important features to dynamic power
  - Correlate to per-pattern V_{min} decided by fail logs
- **If power is the root cause:**
  - Linear correlation
  - Outlier patterns have the highest values of power metrics

No.2
Global Dynamic Power

Six power metrics

- Scan cell transitions during loading patterns
- Scan cell transitions during unloading patterns
- Average of WSA per capture cycle
- WSA in the peak capture cycle
- Average of state element transitions per capture cycle
- State element transitions in the peak capture cycle

No.2
Global Dynamic Power



No Correlation Found

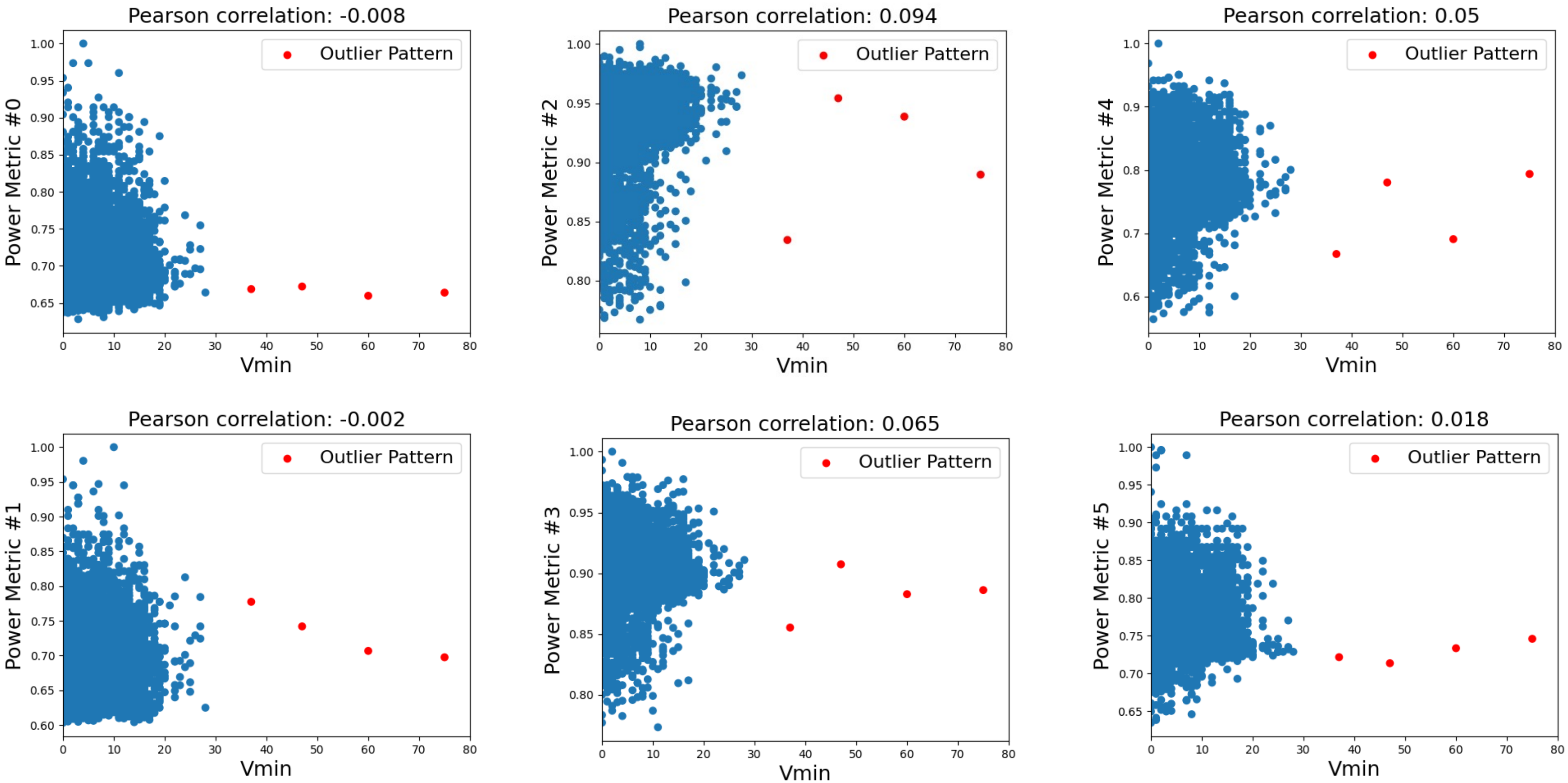
No.3
Local Dynamic Power

- **Hypothesis:**
  Local dynamic power is correlated to V_{min}
- **Experiment:**
  Split the core into several physical grids
  - Calculate per-pattern power metrics for each grid
  - Extract the largest value among all grids

Pattern Id: 1

30.3%	31.2%	33.7%
27.2%	28.8%	35.3%
40.5%	34.2%	31.0%

No.3
Local Dynamic Power



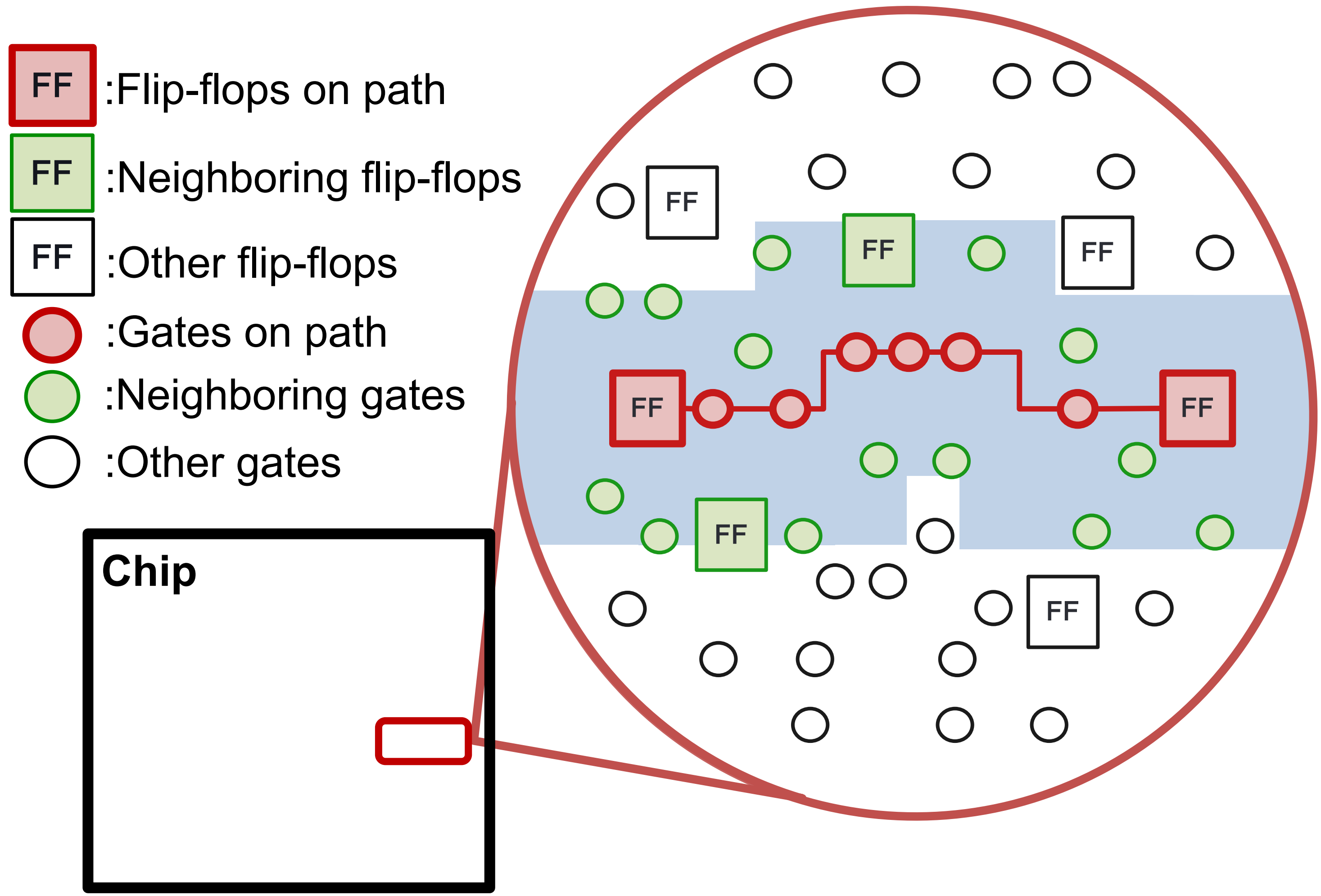
No Correlation Found

No.4
Dynamic Power around the Long Path

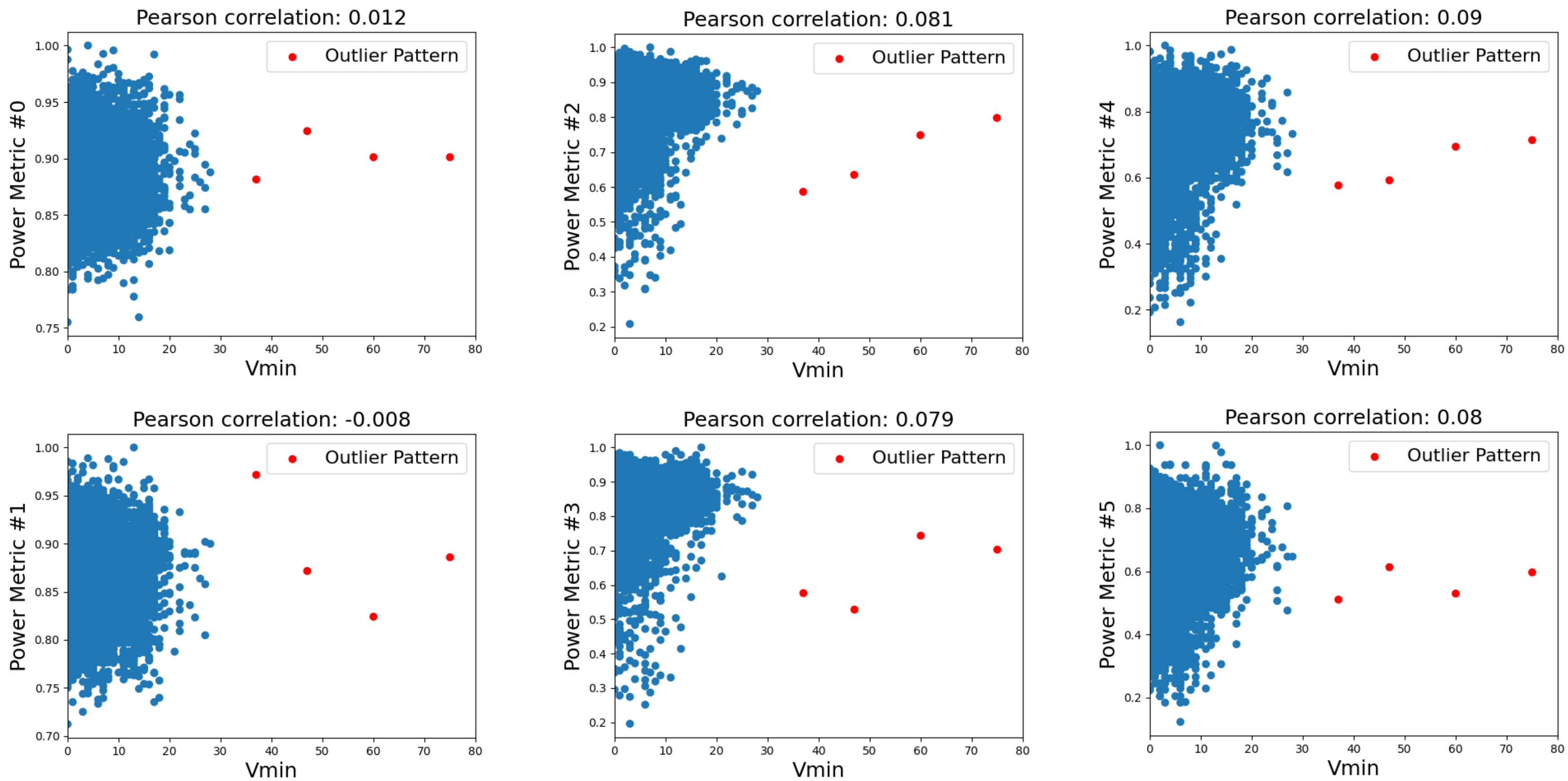
- **Hypothesis:**
  Dynamic power around the longest path is correlated to V_{min}

- **Experiment:**
  Find physically neighboring flip-flops and gates
  - Choose longest path from diagnosis report
  - The longest path is the most suspicious suspect
  - Calculate power metrics around the path

No.4
Dynamic Power around the Long Path



No.4
Dynamic Power around the Long Path



No Correlation Found

No.5
Unconstrained Paths

- **Hypothesis:**
  The longest path is timing critical
- **Experiment:**
  Report the timing of the longest path
  - With PrimeTime
  - The path is unconstrained path which should not be activated
  - Each outlier pattern activates at least one unconstrained path
- **Apply path delay fault simulation**
  - Unconstrained path delay faults are detected
- **Apply one-hot patterns**
  - Validate that unconstrained paths are the root cause

Path Delay Fault Simulation

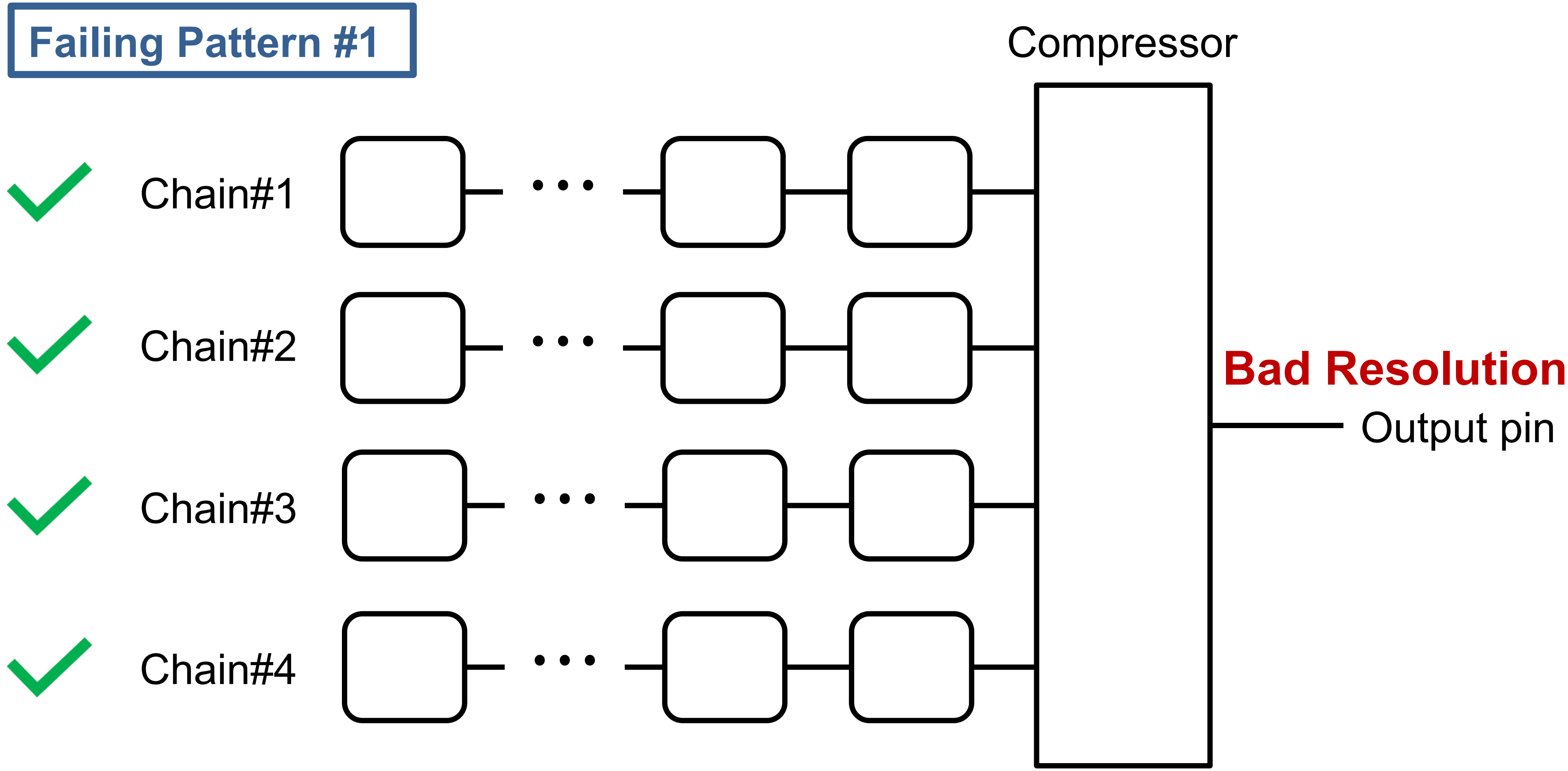
- **Require path definition file**
  - Contain each pin on the paths
- **Unconstrained paths should not be activated**
  - If a path delay fault is detected
    → The path is activated
- **Simulation Results**
  - Some unconstrained paths are activated

Example of path definition file:

```
Path "path1" =
  Pin FF1;
  Pin Gate1;
  Pin Gate2;
  Pin Gate3;
  Pin Gate4;
  Pin FF2;
End;
Path "path2" =
        ⋮
```

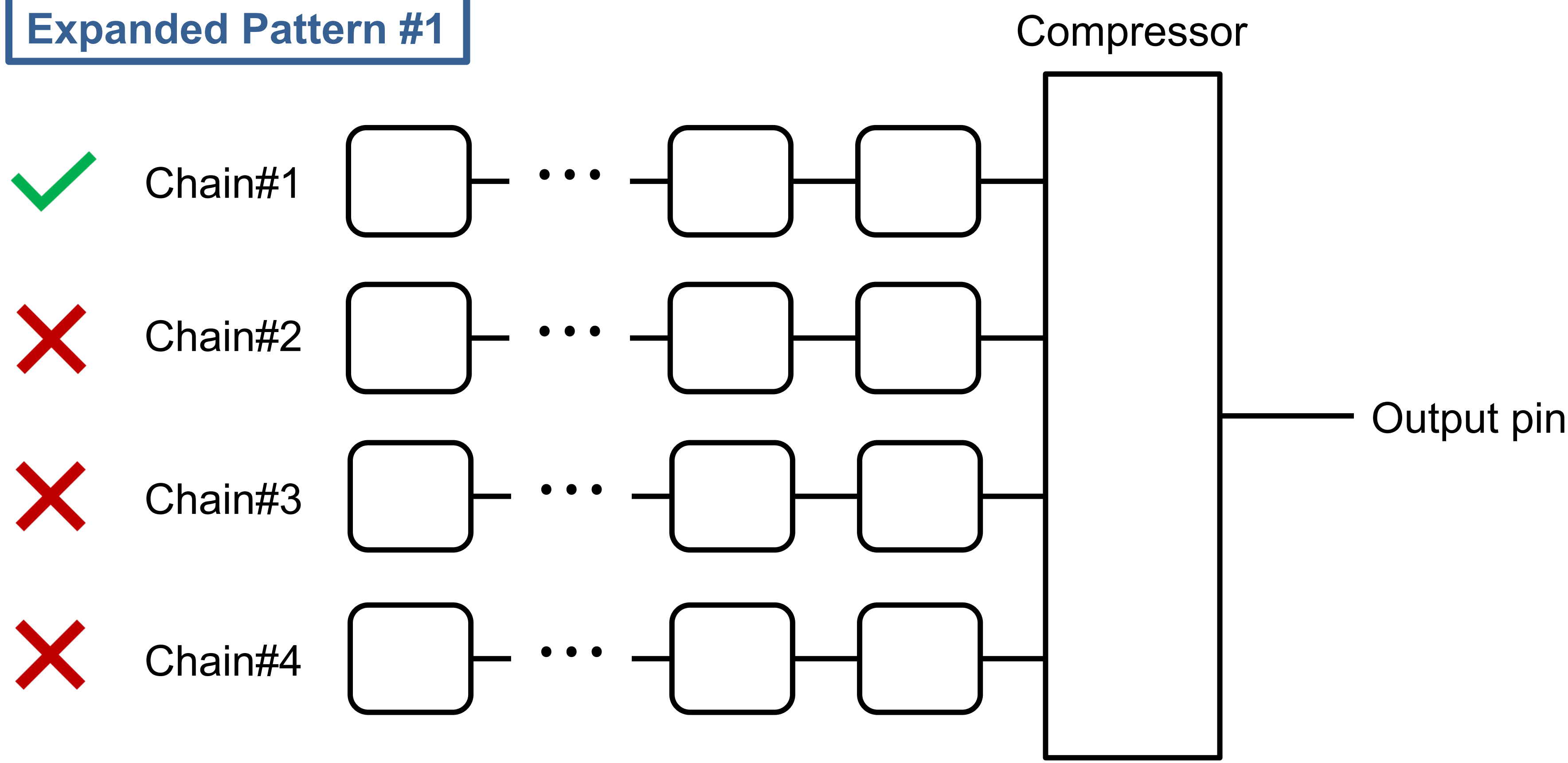
One-hot Patterns (1/3)

Failing Pattern #1



One-hot Patterns (2/3)

Expanded Pattern #1



One-hot Patterns (3/3)

- **Expand an outlier pattern to a set of one-hot patterns and apply it on ATE**
  - The suspected unconstrained path still exist
  - Very high possibility that unconstrained paths are the root causes of outlier patterns
- **Debug conclusion**
  - Unconstrained paths are very likely to be the root causes of outlier patterns

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Prevention Methods

- **To prevent test pattern from capturing the responses of unconstrained paths**
  - Maintain the same fault coverage
- **Pre-silicon and post-silicon methods**
  - Independent
  - Post-silicon can be applied after pre-silicon if desired

Methods Comparison

Pre-silicon method

- Don’t require ATE test results
- Require path definition file from SDC
- Require path delay fault simulation
- More pattern count inflation

Post-silicon Method

- Require ATE test results
- Less pattern count inflation

Extract Paths from SDC

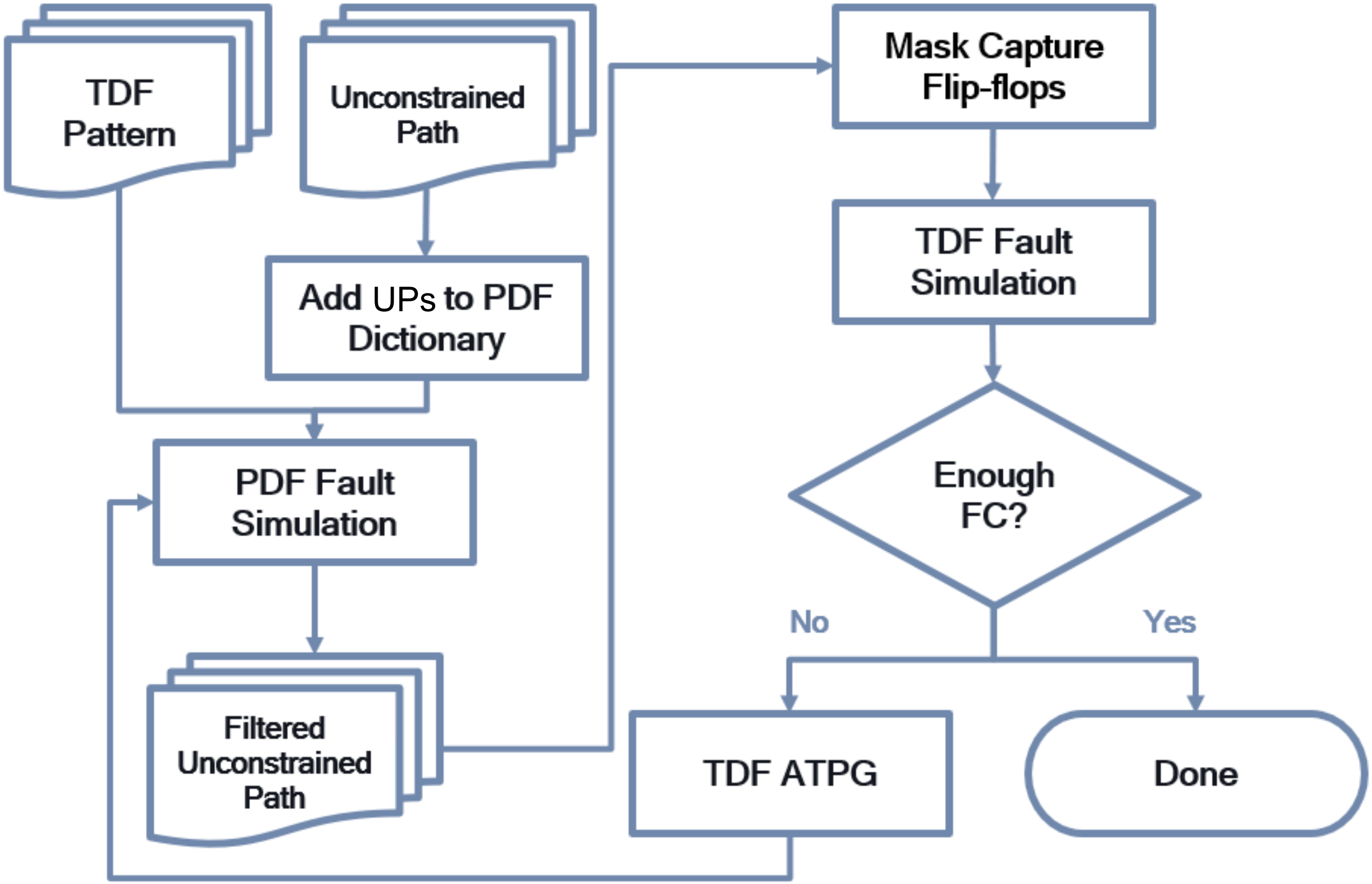
SDC file

```
set_false_path
-from A -to B

set_false_path
-from C -to D

set_multicycle_path
-from E -to F

set_multicycle_path
-from G -to H
```

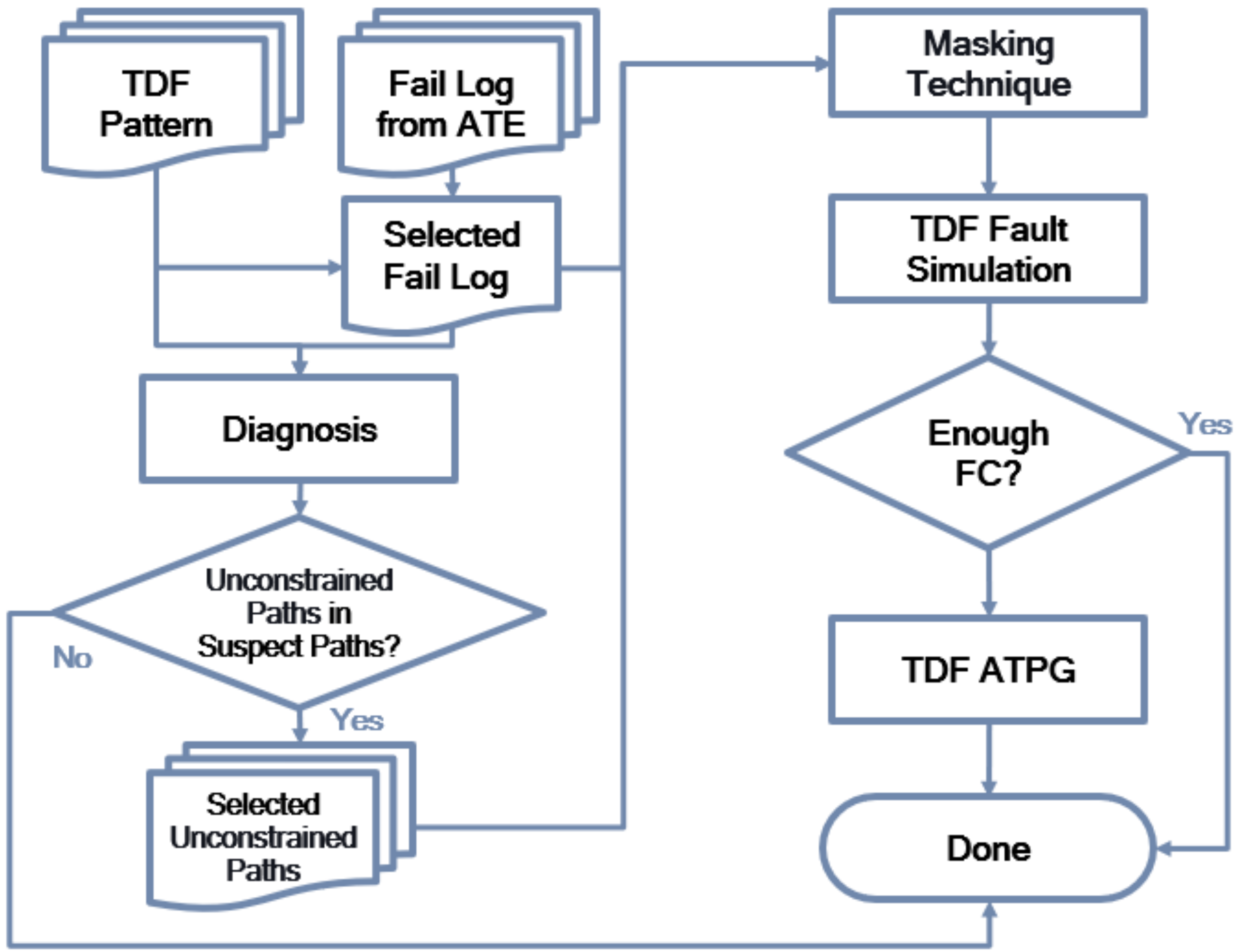
Path Definition file

```
Path “path1” =
  Pin A;
  Pin B;
End;
Path “path2” =
  Pin C;
  Pin D;
End;
Path “path3” =
  Pin E;
  Pin F;
End;
Path “path4” =
  Pin G;
  Pin H;
End;
```

Pre-silicon Method



Post-silicon Method



Masking Technique

1. **Mask capture flip-flops for all patterns**
   - Avoid capture responses of unconstrained paths
   - Better diagnostic information
   - Apply on all patterns

2. **Mask failing cycles for outlier patterns**
   - Directly ignore the failing cycles based on fail logs
   - Worse diagnostic information
   - Apply on outlier patterns only

Masking Technique

Pattern ID	Flip-Flop ID	String	Pass or Fail	Masking Tech. 1	Masking Tech. 2
Pattern A	1	H	F	X	X
	2	L	P	L	L
	3	H	P	X	H
Pattern B	1	L	P	X	L
	2	L	P	L	L
	3	H	P	X	H
Pattern C	1	L	P	X	L
	2	H	P	H	H
	3	L	F	X	X
Pattern D	1	L	P	X	L
	2	H	P	H	H
	3	H	P	X	H
Pattern E	1	H	F	X	X
	2	H	P	H	H
	3	L	F	X	X

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Experiment Data

- **Debugging results of PS and PS_{13}**
  - Pre-silicon and post-silicon methods
- **Experiments on 12 chips**
- **Evaluation metrics**
  - Pattern count inflation
  - V_{min} improvement

Pre-silicon Method Results

- Significant V_{min} improvements
- Pattern count inflation is low compared to low power pattern sets

Pattern Set	Pattern Count Inflation (%)	Pattern-set V_{min} Improvement (mV)	
		μ	σ
PS'	0.33	30.17	12.25
PS'_{13}	0.50	39.33	8.02

Post-silicon Method Results

- Significant V_{min} improvements
- All pattern sets have lower pattern count inflation compared to pre-silicon method

Pattern Set	Pattern Count Inflation (%)	Pattern-set V_{min} Improvement (mV)	
		μ	σ
PS''	0.04	28.83	11.74
PS'''	0	29.17	11.58
PS''_{13}	0.24	35.50	5.33
PS'''_{13}	0	35.17	5.42

Comparison

- V_{min} **improvements**
  - Pre-silicon methods has a little more V_{min} improvements than post-silicon method
  - Post-silicon method with either masking techniques has similar V_{min} improvements
- **Pattern count inflation**
  - Pre-silicon methods has the largest pattern count inflation
  - Post-silicon with masking cycles has the least pattern count inflation

Overall Comparison

	Need ATE	Need PDF Simulation	V_{min} Improvement	Pattern Count Inflation	Diagnostic Information
Pre-silicon	No	Yes	1^{st}	3^{rd}	-
Post-silicon with masking technique1	Yes	No	2^{nd}	2^{nd}	1^{st}
Post-silicon with masking technique2	Yes	No	2^{nd}	1^{st}	2^{nd}

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Conclusion

- **Debug the root cause of abnormally high V_{min} pattern set to be unconstrained paths**
- **Propose pre-silicon and post-silicon methods to prevent high V_{min} patterns caused by unconstrained paths**
  - Achieve 28.83mV to 39.33mV V_{min} improvements
  - Only 0% to 0.5% pattern count inflation

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- **Thanks to the following Qualcomm staff**
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  - Subhadip Kundu
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  - Bing-Han Hsieh
  - Khee Sang Cheah

Qualcomm

Thank you!

References

- [Pant 09] P. Pant and J. Zelman, "Understanding Power Supply Droop during At-Speed Scan Testing," 2009 27th IEEE VLSI Test Symposium
- [Srivastava 22] A. Srivastava and J. Abraham, "Low Capture Power At-Speed Test with Local Hot Spot Analysis to Reduce Over-Test," 2022 IEEE International Test Conference (ITC)
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- [Kim 03] Kee Sup Kim, S. Mitra and P. G. Ryan, "Delay defect characteristics and testing strategies," Design & Test of Computers, 2003

Thank you for listening!

Any question?

APPENDIX

Run Time

Debug	Time	Machine
Pattern Generation	~28 hours	gridsdca
Power Analysis Global	~5 hours	gridsdca
Power Analysis Local - Grid	~7 days	gridsdca
Power Analysis Local - Path	~7 days	gridsdca
Diagnosis	~5 hours	gridsdca
Prevention Methods	**Time**	**Machine**
Generate Path Definition File	~45 hours	ecdca
Pre-Silicon Method	~8 days	gridsdca
Post-Silicon Method FF	~20 hours	gridsdca
Post-Silicon Method Cycle	~13 hours	gridsdca